BARRIER METAL LAYER FOR A CARBON NANOTUBE FLAT PANEL DISPLAY

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of U.S. Application No. 10/226,405, filed August 22, 2002, which is incorporated by reference in its entirety.

BACKGROUND

Field of the Invention

[0002] The present invention relates to electron-emitting devices, such as those for use in field emissive display devices, and in particular to forming electron-emitting devices using a barrier material.

Background of the Invention

[0003] A Cathode Ray Tube (CRT) display generally provides the best brightness, highest contrast, best color quality and largest viewing angle of prior art computer displays. CRT displays typically use a layer of phosphor, which is deposited on a thin glass faceplate. These CRTs generate a picture by using one to three electron beams, which generate high-energy electrons that are scanned across the phosphor in a raster pattern.

[0004] The phosphor converts the electron energy into visible light so as to form the desired picture. However, prior art CRT displays are large and bulky due to the large vacuum envelopes that enclose the cathode and extend from the cathode to the faceplate of the display. Therefore, typically, other types of display technologies such as active matrix liquid crystal display, plasma display and electro-luminescent display technologies have been used in the past to form thin displays.

[0005] Recently, a thin flat panel display (FPD) has been developed which uses the same process for generating pictures as is used in CRT devices. These flat panel displays use a backplate including a matrix structure of rows and columns of electrodes. One such flat panel display is described in U.S. Patent No. 5,541,473, which is incorporated herein by reference. Flat panel displays are typically matrixed-addressed and they comprise matrix-addressing electrodes. The intersection of each row line and each column line in the matrix defines a pixel, the smallest addressable element in an electronic display.

[0006] The essence of electronic displays is the ability to turn on and off individually picture elements (pixels). A typical high information content display will have about a quarter million pixels in a 33 cm diagonal orthogonal array, each under individual control by the electronics. The pixel resolution is normally just at or below the resolving power of the eye. Thus, a good quality picture can be created from a pattern of activated pixels.

[0007] One means for generating arrays of field emission cathode structures relies on well-established semiconductor micro-fabrication techniques. These techniques produce

highly regular arrays of precisely shaped field emission tips. Lithography, generally used in these techniques, involves numerous processing steps, many of them wet. The number of tips per unit area, the size of the tips, and their spacing are determined by the available photoresists and the exposing radiation.

[0008] Tips produced by the method are typically cone-shaped with base diameters on the order of 0.5 to 1 μm, heights of anywhere from 0.5 to 2 μm, tip radii of tens of nanometers. This size limits the number of tips per pixel possible for high-resolution displays, where large numbers (400 - 1000 emitters per pixel) are desirable for uniform emission to provide adequate gray levels, and to reduce the current density per tip for stability and long lifetimes. Maintaining two-dimensional registry of the periodic tip arrays over large areas, such as large TV-sized screens, can also be a problem for gated field emission constructions by conventional means, resulting in poor yields and high costs.

[0009] U.S. Pat. No. 4,338,164 describes a method of preparing planar surfaces having a microstructured protuberances thereon comprising a complicated series of steps involving irradiation of a soluble material (e.g., mica) with high energy ions, as from a heavy ion accelerator, to provide column-like traces in the matrix that are subsequently etched away to be later filled with an appropriate conductive, electron-emitting material. The original soluble material is then dissolved following additional metal deposition steps that provide a conductive substrate for the electron emitting material. The method is said to produce up to 10^6 emitters per cm^2, the emitters having a diameter of approximately 1 - 2μm.

[0010] U.S. Pat. 5,266,530, incorporated by reference, describes a gated electron field emitter prepared by a complicated series of deposition and etching steps on a substrate, preferably crystalline.

[0011] FIG. 1 is a prior art flat CRT cathode of tungsten as a thermionic electron source placed on a substrate. Scan electrons and data electrodes are formed on a glass plate having a plurality of holes at pixel locations. The electrodes with predetermined voltages applied thereto selectively pass the electrons emitted from the line cathode so that the electrons accelerate toward a screen and excite phosphors coated on the inner surface of the screen. Different types of emitters have been suggested in the past for the flat CRT shown in FIG. 1.

[0012] Among these different emitters is the use of carbon nanotubes. In the carbon nanotube displays, microstructures are disposed on a row electrode so that when voltage is applied to between the row electrode and a column electrode, electrons are emitted from the cathode to the screen to excite the phosphors on the screen to create images.

[0013] FIG. 2 shows a schematic (cross-sectional view) of a portion of a prior art matrixed addressed ungated field emission display device 10 including cathode 20, for one embodiment of the invention. Patterned microstructure layer 12 disposed on row conductors 16 which are supported by substrate 14 provides cathode 20. Transparent column conductors 18, generally indium tin oxide (ITO), are disposed on substrate 22, which may be glass. The faceplate supports a layer of continuous or discontinuous phosphor material 23 and which comprises anode 24 of the invention. Phosphor material 23 is capable of excitation by electrons. Upon applying a voltage from voltage

source 26, there results a high electric filed being applied to the emission sites of microstructured layer 12. This causes a flow of electrons across low-pressure gas or vacuum gap 28 between column conductors 18 and row conductors 16.

[0014] FIG. 3 is another prior art example of a gated matrixed addressed field emission display device 30. The device includes a gated cathode 32 which includes a conductive gate columns 34, insulated spacers 36, patterned microstructured layer 38, deposited on and in electrical contact with row conductors 40 which are supported on substrate 41, generally glass. Cathode 32 is spaced apart from anode 42 by low-pressure gas or preferably vacuum gap 44, the space between phosphor 50 and cathode 32. Anode 42 includes substrate 46 on which is located a transparent phosphor containing layer 50.

[0015] FIG. 4 shows a cross sectional view of a portion of a prior art carbon nanotube CRT display. The display in FIG. 4 includes a gated cathode, a patterned microstructure layer consisting of carbon nanotube structures, insulated spacers, a patterned microstructure layer deposited on it and electrical contact with row conductors that are supported on the substrate. Cathode is spaced apart from an anode structure by a low-pressure vacuum. The anode comprises a faceplate, a conductor layer and phosphor which when bombarded with electrons emitted from the cathode excites the phosphor. The nanotube structure shown in FIG. 4 typically includes a resistive layer between the cathode conductors and the microstructure emissive elements. The microstructure emissive elements and the resistive layer are typically constructed in a planar configuration.

[0016] FIG. 5 is another example of a carbon nanotube field emission display device of the prior art. The field emitter of FIG. 5 illustrates a multilayer structure 300 which is a cross sectional view of a portion of an FED flat panel display. The multi-layer structure 100 comprises a field emission backplate structure 110. An image is generated at faceplate structure 160.

[0017] The backplate structure 110 generally comprises of a patterned emitter electrode 120, a resistive layer 115, an electrically insulating layer 140, a gate layer 150 and electron-emissive elements 140 situated in an aperture through insulating layer 135. The electron-emissive elements 140 are carbon-based material.

[0018] The backplate 110 also includes a catalyst layer upon which the electron-emissive elements 140 are situated. The resistive layer 115 and the catalyst layer 120 give the structure 100 the uniformity of emitter elements formation that is required to generate the proper imagery in the display. Although the structure 100 shown in FIG. 5 has a vertical structural construction, the catalyst layer and the resistive layer 115 may be fabricated to be planar.

[0019] It is typical in the prior art device shown in FIG. 5 to have a nickel (Ni) material as the catalyst layer and a silicon-based material (Si) as the resistive layer 115. The catalyst material, in this case Ni, interfaces directly with the resistive layer 115. The interfacing between the catalyst 120 and resistive layer 115 materials results in a poly-crystallization process from the inter-diffusion between the catalyst material and the resistive layer 115 material. The poly-crystallization process often results in lowering the resistive value of the resistive layer 115. The poly-crystallization of the Ni catalyst

and the Si resistor also affects the adhesion capabilities of catalyst layer. As the catalyst layer diffuses into the resistive layer 115, the catalyst layer loses the ability to act as an effective adhesion layer between the emitter elements 140 and the resistive layer 115. Weakening the adhesion capabilities of the catalyst layer makes it difficult to grow the emitter elements 140 and results in a costly fabrication process.

SUMMARY OF THE INVENTION

[0020] To avoid the deficiencies in existing devices, an electron-emitting device includes a barrier layer between an emitter electrode structure and a catalyst layer, upon which microstructures of carbon nanotubes are formed. The barrier layer thus acts as an anti diffusion layer between the catalyst layer and the emitter electrode structure. Specifically, for example, the barrier layer may be disposed between the catalyst layer and a resistive layer of the emitter electrode structure. In this way, the catalyst layer may be prevented from diffusing into the resistive layer before the growing of the carbon nanotubes or other electron-emissive elements. The barrier layer may also enhance the adhesion characteristics of the catalyst layer to improve the uniformity of growth of the electron-emissive elements with the catalyst layer.

[0021] In one embodiment, an electron-emitting device includes an emitter electrode structure, a barrier layer disposed at least partially over the emitter electrode structure, and a catalyst layer disposed at least partially over the barrier layer, the catalyst layer for forming a plurality of electron-emissive elements electrically coupled to the emitter electrode structure. The emitter electrode structure may include an emitter electrode and a resistive layer disposed over the emitter electrode, where the barrier layer is disposed between the resistive and catalyst layers.

[0022] In another embodiment, the electron-emitting device is used in a field emission display device, which comprises a matrix of pixels, each pixel having one or more colors. For each color of each pixel, an electron-emitting device is configured to direct electrons towards a phosphor in the display device.

[0023] In one embodiment, an electron-emitting device includes a metal barrier layer with a plurality of laterally separated sections situated between electron-emissive elements, on one hand, and an emitter electrode structure, on the other hand. These sections of the barrier layer may be situated under corresponding sections of a catalyst layer, which are likewise spaced apart along the emitter electrode.

[0024] The display may further include an electric field producing structure that comprises first and second conductive electrodes insulatively spaced apart and substantially parallel to each other. The first conductive electrode comprises a layer of electron emitting elements, preferably made of carbon nanotube, a resistive layer, a catalyst layer to provide emitter distribution uniformity, and a barrier layer that acts as an adhesive layer between the catalyst layer and the resistive layer. The barrier layer also acts as an anti-diffusion layer between the resistor and the catalyst layers.

[0025] In one embodiment, a method for forming an electron-emitting device includes the steps of forming a resistive layer over at least a portion of an emitter electrode; forming a barrier layer over at least a portion of the resistive layer; forming a catalyst layer over at least a portion of the resistive layer, the catalyst layer for forming a plurality of electron-emissive elements; and forming the electron-emissive elements using the catalyst layer, the electron-emissive elements electrically coupled to the emitter electrode structure.

[0026] In another embodiment for making an electron-emitting device, the device includes a cathode structure that includes, electrically coupled in series, an emitter electrode, a resistive layer, and a plurality of electron-emissive elements. To form the

device, at least the following steps are performed in either order but before the electron-emissive elements are formed: (a) an electrically conductive barrier material is disposed on at least a portion of the resistive layer; and (b) a catalyst material is disposed on at least a portion of the barrier material so that at least some of the catalyst material is physically isolated but electrically coupled to the resistive layer.

[0027] In some embodiments for making the electron-emitting device, a method for making the device may eliminate the need for an extra masking step to provide an initial patterning to the catalyst layer. In such embodiments, the desired pattern can be provided in the barrier layer without increasing the number of masking steps.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] FIG. 1 is a cross sectional view illustrating a prior art flat CRT display device.

[0029] FIG. 2 is a cross sectional view illustrating a prior art matrixed addressed ungated field emission display device.

[0030] FIG. 3 is a cross sectional view illustrating a prior art matrixed addressed gated filed emission display device.

[0031] FIG. 4 is a cross sectional view illustrating a prior art carbon nanotube display device.

[0032] FIG. 5 is a cross sectional view illustrating a prior art carbon nanotube field emission display device.

[0033] FIG. 6A is one embodiment of the carbon nanotube field emission display device of the present invention.

[0034] FIGS. 6B through 6G are cross sectional structural views represent steps in manufacturing an embodiment of the carbon nanotube electron emitting device of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0035] Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, in view if this disclosure it will be appreciated by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

[0036] FIG. 6A illustrates the core of a matrix-addressed field emitter that contains an emitter conductor patterned into conductor strips in a vertically aligned manner according to the invention. The cross sections of FIG. 6A is taken through perpendicular planes. The field emitter of FIG. 6A is created from a flat electrically insulating baseplate (substrate) 600 typically consisting of glass having a thickness of approximately 1 mm. To simplify the pictorial illustration, baseplate 600 is not shown in the perspective view of FIG. 6A.

[0037] A group of generally parallel emitter electrodes 610 are situated on baseplate 600 as shown in FIG. 6B. Emitter electrodes 610 extend in the row direction and

constitute row electrodes. Alternatively, the emitter electrodes 610 can extend in the column direction and constitute column electrodes. As shown in FIG. 6B, each emitter electrode 610 has a transverse profile roughly in the shape of an upright isosceles trapezoid. This profile helps improve step coverage of layers formed above emitter electrodes 610.

[0038] Emitter electrodes 610 typically consist of aluminum, molybdenum, chromium, or an alloy of any of these metals; however, a variety of different metals or other materials could be used in the emitter electrodes 610. In one embodiment, the emitter electrode 610 is about 1000 to 5000 Å in thickness.

[0039] In one embodiment of the present invention, the emitter electrode 610 is deposited in-situ by a number of well known deposition methods of the prior art. In one embodiment. Sputter deposition may be used.

[0040] Upon deposition of the emitter electrode 610, a photo-resistive mask agent (PR) masks the emitter electrode 610 according to a designed pattern. The photo-resistive mask is then soft baked. After masking and baking the photo-resistive mask, the emitter electrode 610 is etched by a number of photolithographic processes well known in the art accordingly. Applicable etching methods include wet etching. Remaining PR maskant is stripped off by methods well known in the art.

[0041] A resistive layer 620 is then fabricated by deposition of a layer of resistive material on the emitter electrode layer 610 and remaining surfaces of the glass 600 uncovered by the emitter electrode 610 material as shown in FIG. 6C. In one embodiment of the present invention, the resistive layer 620 is formed like an island at

each pixel along the surface of the emitter electrode 610. In one embodiment of the present invention, the resistive layer 620 is deposited by a number of well-known methods in the art. In one embodiment, deposition of the resistive layer 620 is accomplished by plasma enhanced chemical vapor deposition (PECVD) method.

[0042] Upon deposition of the resistive layer 620, a photo-resistive masking agent (PR) masks the resistive layer 620. After masking, the resistive layer 620 is soft baked and exposed. The resistive layer 620 is subsequently developed by hard baking and dry etching to conform to the contours of the surface of the glass 600. Remaining PR maskant is stripped by methods well known in the art. In another embodiment, resistive layer 620 can be patterned at the same time and with the same pattern as the barrier layer 640.

[0043] A patterned barrier layer 640 and a catalyst layer 650 are then fabricated by depositing the layers on the resistive layer 620 as shown in FIG. 6D. In one embodiment of the present invention, the barrier layer 640 is deposited by a number of well-known methods in the art. In one embodiment, deposition of the barrier layer 640 is accomplished by the use of a sputter deposition method. In one embodiment of the present invention, the barrier layer is formed of titanium tungsten (TiW). Alternatively, the barrier layer may be formed of titanium nitride (TiN), tungsten (W), tungsten nitride (WN), chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum nitride (TaN), or a combination of any of these metals with another material, for example, as an alloy including one or more of these metals.

[0044] In one embodiment of the present invention, the barrier layer 640 acts as an anti-diffusion layer between the resistive layer 620 and a catalyst layer upon which the

carbon nanotube emissive elements of the present invention are formed or grown. The barrier layer 640 thus protects the catalyst layer material from diffusing into the resistive layer 620. In another embodiment of the present invention, the barrier layer 640 enhances the adhesion capabilities of the catalyst layer 650 to enable the carbon nanotube electron emissive elements to adhere to the catalyst layer 650.

[0045] In one embodiment, the catalyst layer 650 and the barrier layer 640 are disposed as a group of laterally separated sections coupled to the emitter electrode 610 by the resistive layer 620, as shown in FIG. 6E. The catalyst layer 650 facilitates the formation of carbon nanotube or other electron-emissive elements thereon. The sections of the catalyst layer 650 extend in the column direction and are spaced apart along each emitter electrode 610. The catalyst layer 650 may effectively be a conductor in that current flows through the catalyst layer 650 largely in the vertical direction between electrode 610 and the overlying electron-emissive elements described below.

[0046] The catalyst layer 650 typically comprises nickel, iron, cobalt, or the alloys of these metals. In one embodiment, the thickness of the catalyst layer is between 1 nm and 200 nm.

[0047] As shown in FIG. 6F, a blanket dielectric layer 630 is formed or deposited on the surface of the catalyst layer 650 and the resistive layer 620 covering at least portions of the resistive layer 620 that are left uncovered by the barrier layer 640. In another embodiment, the resistive layer 620 is sectioned along with the barrier layer 640 and the catalyst layer 650. In another embodiment, the catalyst layer 650 is not deposited until after the dielectric layer 630 and gate electrode 660 are formed. The dielectric layer 630 typically includes of silicon oxide having a thickness of 0.5 to 2.5 μm. In another

embodiment, the dielectric layer 630 includes silicon nitride having a thickness of 0.5 to 2.5 μm. However, the dielectric layer 630 can be formed of any suitable electrically insulating material depending on the intended application.

[0048] A blanket electrically conductive gate layer 660 is formed on dielectric layer 630, as also shown in Fig 6G. Gate layer 660 is typically created by sputter depositing a metal such as chromium or aluminum over dielectric layer 630, although other known techniques can be used to form the gate layer 660. In one embodiment, a passivation or protective layer 670 is formed over the gate layer 660. The passivation layer 670 may comprises silicon oxide, silicon nitride, silicon oxinitride, or other suitable material, helping to seal or protect the structure from corrosion or other damage.

[0049] A photoresist mask bearing the pattern intended for the main control portions is formed on gate layer 660. The exposed portions of gate layer 660 are removed with a chemical etchant. Alternatively, a plasma can be employed to remove the exposed portions of layer 660. The patterned remainder of layer 660 consists of a group of laterally separated main control portions extending in the row direction.

[0050] An array of rows and columns of main control openings 680 extend through main control portions 660 down to dielectric layer 630. One main control opening 680 is provided for each set of electron-emissive elements 690. In particular, one main control opening 680 is present at each location where a main control portion 660 crosses over an emitter electrode 610.

[0051] Gate openings that implement control openings 680 are formed at multiple locations through each of the portions of gate layer 660 that span main control openings

680. Using gate layer 660 as an etch mask, the dielectric layer 630 is etched through gate openings 680 to form dielectric openings. FIG. 6A shows the resultant structure.

[0052] Electron-emissive elements 690 are formed in composite openings 680. Various techniques can be employed to create the carbon nanotubes 690.

[0053] During field emitter operation, the voltages on electrodes 610 and 660 are controlled in such a way that control electrodes 660 extract electrons from electron-emissive-elements 690 in selected ones of the electron-emissive element sets. An anode in the light-emitting device (not shown here) situated opposite elements 690 draws the extracted electrons towards light-emissive elements located close to the anode. As electrons are emitted by each activated electron-emissive element 690, a positive current flows from the electron-emissive elements 690 to the underlying emitter electrode 610.

[0054] A sectioned catalyst layer 650 provides the field emitter with electron emission uniformity and short circuit protection. Specifically, if sectioned, the catalyst layer 650 limits the maximum current that can flow through activated electron-emissive elements 690. Since the positive current flowing through each activated element 690 equals the electron current supplied by that element 690, the sectioned catalyst layer 650 limits the number of electrons emitted by activated elements 690. This prevents some of elements 690 from providing many more electrons than other of elements 690 at the same extraction voltage and thus prevents undesirable bright spots from occurring on the viewing surface of the flat-panel display.

[0055] Also, if one of gate electrodes 660 becomes electrically shorted to an underlying conductor and thus becomes electrically coupled to underlying emitter

electrode 610, the catalyst layer 650 at the short circuit location significantly limits the current flowing through the short circuit connection. The vertical conductance of the catalysts layer 650 at the short circuit location is so high that substantially the entire normal voltage drop between electrodes 660 and 610 at the short circuit location occurs across the intervening portion of the catalyst layer 650. With proper electron-emitter design, the presence of the short circuit does not detrimentally affect the operation of any of the other sets of electron-emissive.

[0056] Such a short circuit can arise by way of a conductive path created through a dielectric layer 630 or by having one or more of electron-emissive elements 690 come into contact with their gate electrode 660. In the case of a control electrode-to-electron-emissive-element short circuit, each shorted electron emissive element 690 is normally defective. However, the catalyst layer 650 limits the current through each shorted elements 690 sufficiently that non-shorted elements 690 in that set of electron-emissive elements normally still operate in the intended manner. The catalyst layer 650 thus normally enables a set of electron emissive elements 690 containing a small percentage of shorted elements 690 to perform the intended electron-emitting function in an adequate manner. Electron-emission uniformity is substantially maintained.

[0057] The electron emitters produced according to the invention can be employed to make flat-panel devices other than flat-panel CRT displays. Likewise, the present electron emitters can be used as electron sources in products other than flat-panel devices. Various modifications and applications may thus be made by those skilled in the art without departing from the true scope and spirit of the invention as defined in the appended claims.